ground power supply voltage GND. The sources of transistors D2 and D3 are connected to node VBUM. Other clamping circuits other than the one depicted also may be used with the comparator of the present invention.

In addition, a hysteresis circuit **28**, known to those of ordinary skill in the art, may be used to reduce the susceptibility of the comparator to noise from other components. Hysteresis circuit **28** includes transistors H1–H3. Transistors H1 and H2 are p-channel MOSFETs, and transistor H3 is an n-channel MOSFET. Transistor H1 has its source connected to power supply voltage V_{CC}. The gate of transistor H1 is connected to the gate and source of transistor **M16**. The gate of transistor H2 is controlled by the output of inverter **34**; the gate of transistor H3 is controlled by the output of inverter **32**. Inverters **32** and **33** are the same as inverters **10** and **12**.

As a result, a DCSBV comparator provides an indicator for switching between a primary and secondary power supply without requiring a large number of devices for implementation as compared to a typical bandgap reference circuit. The present invention eliminates the need for using a large number of bipolar devices, large resistors, oscillators, switch capacitors, auto zero devices, etc. Through the use of current mirrors, the number of bipolar devices required are reduced. Additionally, sensitivity to noise also may be reduced by using a DCSBV comparator according to the present invention.

Although the depicted embodiment employs for current mirrors, other numbers of current mirrors and current mirrors of other designs may be used as long as the implementation of the current mirrors performs the function of summing currents at a node. Additionally, more than one node may be used for summing currents.

An example of typical values which can be used to fabricate an operational device are as follows. These numbers assume a typical processing technology, and a desired trip point for the comparator of approximately 4.4 volts. The constants K_1, K_2, and K_3, respectively, can be set to the values 2, 7, and 46 by proper selection of the various components and transistor sizes. Transistor design to give current densities of J_1=1.0 A/cm^2 and J_2=0.05 A/cm^2 provides for operation as described above.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor length in the first, second, and third current sources, respectively; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node.

2. The direct current sum bandgap voltage comparator of claim **1**, wherein the plurality of current sources are current mirrors.

3. A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node, wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor length in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprises four current mirrors.

4. The direct current sum bandgap voltage comparator of claim **3**, wherein the first current mirror includes a plurality of transistors and supplies a current to the summing node defined by $K_1(V_{CC}-V_T)$.

5. The direct current sum bandgap voltage comparator of claim **4**, wherein the second current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_1V_T.

6. The direct current sum bandgap voltage comparator of claim **5**, wherein the third current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_2V_{BE}.

7. The direct current sum bandgap voltage comparator of claim **6**, wherein the fourth current mirror supplies a current to the summing node defined by $K_3(kT/q)$.

8. The direct current sum bandgap voltage comparator of claim **7** further comprising a clamping circuit connected to the summing node, wherein a voltage swing for the summing node, responsive to changes in current supplied by the current mirrors, may be set between predetermined voltages.

9. The direct current sum bandgap voltage comparator of claim **7** further comprising a cascode stage having at least a first and second connections, the first connection is connected to the summing node and the second connection is connected to one of the four current mirrors.

10. The direct current sum bandgap voltage comparator of claim **7** further comprising a hysteresis circuit connected to the indicator circuit to reduce noise.

11. The direct current sum bandgap voltage comparator of claim **7**, wherein the indicator circuit includes a pair of

inverters connected in series, wherein an input in the first inverter is the input of the indicator circuit connected to the summing node and an output of the second inverter is the output of the indicator circuit.

12. The direct current sum bandgap voltage comparator of claim 11, wherein the indicator circuit provides a logic one output if the power supply is equal to or greater than a preselected voltage.

13. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor length in the first, second, and third current sources, respectively;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in the summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit if the logical signal indicates that the power supply voltage is equal to or greater than the predetermined threshold voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the predetermined threshold voltage.

14. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source further comprising at least one transistor, and each current source supplying a current to the summing node and being connected to a power supply voltage;

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in the summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit if the logical signal indicates that the power supply voltage is equal to or greater than the preselected voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the preselected voltage, wherein the current sources supply according to a bandgap equation:

$$K_1(V_{CC}-V_T)+K_1V_T=K_2V_{BE}+K_3(kT/q)$$

where V_{CC} is the power supply voltage, V_T is a predetermined threshold voltage of a transistor in a first current source within the plurality of current sources, V_{BE} is a base emitter voltage of a transistor in a second current source within the plurality of current sources, k is Boltzman's constant, T is a temperature in kelvin of a transistor in a third current source within the plurality of current sources, q is an electronic charge constant, and K_1, K_2, and K_3 are constants determined by a resistance and a transistor length in the first, second, and third current sources, respectively, and wherein the plurality of current sources comprises four current mirrors.

15. The zero power circuit of claim 14, wherein the secondary power supply is a battery.

16. The zero power circuit of claim 14, wherein the first current mirror includes a plurality of transistors and supplies a current to the summing node defined by $K_1(V_{CC}-V_T)$.

17. The zero power circuit of claim 14, wherein the second current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_1V_T.

18. The zero power circuit of claim 17, wherein the third current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_2V_{BE}.

19. The zero power circuit of claim 18, wherein the fourth current mirror supplies a current to the summing node defined by $K_3(kT/q)$.

20. The zero power circuit of claim 19 further comprising a clamping circuit connected to the summing node, wherein a voltage swing for the summing node, responsive to changes in current supplied by the current mirrors, may be set between selected voltages.

21. The zero power circuit of claim 19 further comprising a cascode stage located between the summing node and the current mirrors.

22. The zero power circuit of claim 19 further comprising a hysteresis circuit connected to the indicator circuit to reduce noise.

23. The direct current sum bandgap voltage comparator of claim 19, wherein the indicator circuit provides a logic one output if the power supply is equal to or greater than a preselected voltage.

ADD A1

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Add B4